REMARKS

Applicant respectfully requests reconsideration of this application as amended.

The drawings have been objected to under 37 C.F.R. 1.83(a) as not showing every feature of the invention specified in the claims.

Claims 1-18 are pending in this application.

Claims 1, 5-9, 14-16 have been amended.

No claims have been cancelled.

No claims have been added.

Claims 1, 6 and 8 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 17 was rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,708,598 issued to Saito (hereinafter referred to as "Saito").

Claims 1-8 and 14-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Saito in view of U.S. Patent No. 6,002,623 issued to Stave et al (hereinafter referred to as "Stave").

37 C.F.R. 1.83(a) Objection to Drawings

The Examiner has objected to the drawings as not providing support for the "multiplexer" recited in claim 18. To overcome this objection, Applicant is submitting herewith proposed new Figure 2b and is proposing to renumber Figure 2 as Figure 2a, as shown in accompanying red-lined pages of drawings. Although not related to the Examiner's original objection to the drawings, Applicant seeks to take advantage of this opportunity to correct an errant label in Figure 2 (proposed to be renumbered as Figure 2a), as also shown in the accompanying red-lined pages of drawings. Also accompanying the proposed

new Figure 2b and the proposed renumbering of Figure 2 as Figure 2a are minimal amendments to the text of the specification, offered herein. Proposed Figure 2b, the proposed renumbering of Figure 2 as Figure 2a, and the offered amendments to the specification serve to do nothing more than to provide specific illustration of the brief discussion of a multiplexer that was already present in the paragraph starting at line 1 of page 10 in the specification as originally filed. Applicant has added no new matter with the introduction of either Figure 2b or the offered amendments to the specification, and Applicant respectfully requests the Examiner's approval for these amendments.

35 U.S.C. §112 Rejection of Claims 1, 6 and 8

The Examiner has rejected claims 1, 6 and 8 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention due to the lack of antecedent basis for "the voltage level." Claim 1 has been amended to more distinctly provide antecedent basis. Applicant respectfully submits that claims 1-18, as amended, meet the requirements of 35 U.S.C. §112.

35 U.S.C. §102(b) Rejection of Claim 17

The Examiner has rejected claim 17 under 35 U.S.C. §102(b) as being unpatentable over Saito. Applicant respectfully submits that claim 17 is not anticipated by Saito, because Saito does not teach each and every element of Applicant's invention as claimed.

Specifically, Applicant respectfully submits that Saito does not teach at least the sticky latch as set forth in claim 17. The Examiner has asserted that controller 130 of Saito teaches the sticky latch of claim 17. However, Applicant respectfully asserts that nowhere in the discussion of controller 130 (which is

spread throughout columns 8-13 in Saito) is there any mention of controller 130 acting in any way as any kind of latch.

For at least this reason, Applicant respectfully submits that claim 17 is patentably distinguished over Saito, and is in condition for allowance.

35 U.S.C. § 103(a) Rejection of Claims 1-8 and 14-16

The Examiner has rejected claims 1-8 and 14-16 under 35 U.S.C. § 103(a) as being unpatentable over Saito in view of Stave. To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). (MPEP 2143.03).

Applicant respectfully submits that neither Saito nor Stave, either alone or in combination, teaches or suggests the claimed features of Applicant's invention as recited in independent claims 1 and 14, as amended. Neither Saito nor Stave teach the coupling of a first memory cell to a first and a second bit line, the coupling of a second memory cell to a third and a fourth bit line, the coupling of the first and third bit lines to the inputs of a first comparator, and the coupling of the second and fourth bit lines to the inputs of a second comparator.

Applicant respectfully submits that independent claims 1 and 14 are not rendered obvious by any combination of Saito and Stave, and are in condition for allowance. Applicant further respectfully submits that since claims 2-8 and 15-16 depend, either directly or indirectly, from independent claims 1 and 14, respectively, claims 2-8 and 15-16 are also in condition for allowance.

[redacted]

Allowable Subject Matter and Objections to Claims 9-13 and 18

Applicant gratefully acknowledges the Examiner's indication that claims 9-13 and 18 contain allowable subject matter, and that claims 9-13 and 18 would be allowable if rewritten to correct objections previously discussed.

Regarding claims 9-13, claims 9-13 depend, either directly or indirectly, from claim 1, which Applicant has previously asserted is not rendered obvious by any combination of Saito and Stave, and therefore, is in condition for allowance. Also, regarding claim 18, claim 18 depends from claim 17, which Applicant has previously asserted is patentably distinguished over Saito, and therefore, is in condition for allowance. Therefore, Applicant further respectfully asserts that claims 9-13 and 18 are in condition for allowance.

[redacted]

Condition for Allowance

Applicant submits that all rejections have been overcome and the present application is now in condition for allowance. If there are any additional charges or shortages related to the present communication, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: June 26, 2002

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Name of Person Mailing Correspondence

Signature

6/27/02
Date

[redacted]

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the paragraph starting on line 11 of page 8:

[**Figure 2** is a block diagram of another embodiment] **Figures 2a and 2b** are block diagrams of other embodiments of the present invention. Memory array 200 is substantially similar to memory array 100 of Figure 1, and items numbered with 2xx numbers in [Figure 2] Figures 2a and 2b are meant to correspond to items numbered with 1xx numbers in Figure 1. In a manner corresponding to memory array 100, memory array 200 is comprised of address decoder 220, coupled to memory cell 260 within top half 210 by word line 230, and coupled to memory cell 262 within bottom half 212 by word line 232.

In the paragraph starting on line 3 of page 9:

Regardless of the purpose for having a pair of bit lines connected to each of memory cells 260 and 262, in a manner that corresponds to bit lines 170 and 172 of memory array 100 of Figure 1, in Figure 2a, bit lines 270 and 272 are connected to the inputs of comparator circuit 240, and bit lines 274 and 276 are connected to the inputs of comparator circuit 244. Also corresponding to Figure 1, the outputs of comparator circuits 240 and 244 are connected to latches 242 and 246.

In the paragraph starting on line 1 of page 10:

Furthermore, in an embodiment where memory cells are written to and read from using pairs of bit lines to carry data and its [compliment] complement and sense amplifiers are used in reading from memory cells, the sense amplifiers could also be configured to serve as the comparators used as the comparator circuits to test the memory cells. This could be accomplished

through the use of multiplexers to selectively connect and disconnect different ones of the bit lines as needed to allow the sense amplifiers to perform one or the other of these two functions as depicted by the use of multiplexers 280 and 284 in Figure 2b to selectively couple either one or the other of bit lines 270 or 276 to one input on each of comparators 240 and 244, respectively. Otherwise, in an alternate embodiment, the sense amplifiers and the comparators could remain separate components.

In the paragraph starting on line 18 of page 10:

Figure 3 is a block diagram of yet another embodiment of the present invention. Memory array 300 is substantially similar to memory array 200 of [Figure 2] Figures 2a and 2b, and items numbered with 3xx numbers in Figure 3 are meant to correspond to items numbered with 2xx numbers in [Figure 2] Figures 2a and 2b, with exception of the comparator circuits and their associated latches. In a manner corresponding to memory array 200, memory array 300 is comprised of address decoder 320, coupled to memory cell 360 within top half 310 by word line 330, and coupled to memory cell 362 within bottom half 312 by word line 332. Also in a manner corresponding to memory array 200, memory cell 360 is coupled to bit lines 370 and 374, and memory cell 362 is coupled to bit lines 372 and 376.

In the paragraph starting on line 1 of page 11:

Unlike the [embodiment] embodiments depicted in [Figure 2] Figures 2a and 2b, the comparator circuits of Figure 3 are each comprised of a subtracting circuit and a pair of comparators. Bit lines 370 and 372 are connected to the inputs of subtracting circuit 390. Subtracting circuits 390 subtracts the voltage level of one of bit lines 370 from the voltage level of the other of bit lines 372,

and outputs a voltage that represents the difference resulting from the subtraction, which could be either a positive or negative voltage output. This output of subtracting circuit 390 is, in turn, connected to one of the two inputs on each of comparators 340 and 341. Correspondingly, bit lines 374 and 376 are connected to the inputs of subtracting circuit 392, and the output of subtracting circuit 392 is connected to one of the two inputs on each of comparators 344 and 345. The other input on each of comparators 340 and 344 are connected to a high voltage level reference, +vref, and correspondingly, the other input on each of comparators 341 and 345 are connected to a low voltage reference, -vref. The outputs of comparators 340, 341, 344 and 345 are connected to the inputs of latches 342, 343, 346 and 347, respectively.

In the paragraph starting on line 17 of page 11:

Regardless of whether the memory cells of memory array 300 are written to and read from with a pair of bit lines, or each of the two bit lines connected to each cell are meant to be used to perform independent read and write operations, the testing of memory cells 360 and 362 of memory array 300 is carried out in much the same way as was described above for memory cells 260 and 262 in [Figure 2] Figures 2a and 2b. However, the configuration of comparator circuits that are each comprised of a subtracting circuit and a pair of comparators as shown in Figure 3 affords greater ability to control the degree to which the voltages on pairs of bit lines that are being compared may differ from each other. More precisely, by adjusting +vref and -vref, comparators 340 and 344 can be biased to allow the voltage levels on bit lines 370 and 372 to differ to a degree that is adjustable before either comparator 340 or 344 outputs a signal indicating a malfunction. If the difference in voltage levels between bit lines 370 and 372 is such that it rises above +vref, then comparator 340 will

output a signal indicating so to latch 342, and if the difference in voltages levels between bit lines 370 and 372 is such that it drops below -vref, then comparator 344 will output a signal indicating so to latch 346.

1. (Amended) An apparatus, comprising:

a first memory cell coupled to a first bit line and a second bit line;

a second memory cell coupled to a [second] third bit line and a fourth bit line;

an address decoder coupled to the first and second memory cells to enable access to the first and second memory cells; [and]

a first comparator circuit coupled to the first and [second] third bit lines to compare [the] a voltage level on the first bit line with [the] a voltage level on the [second] third bit line at a time when data is output from the first memory cell on the first bit line and from the second memory cell on the [second] third bit line; and

a second comparator circuit coupled to the second and fourth bit lines to compare a voltage level on the second bit line with a voltage level on the fourth bit line at a time when the complement of the data that is output on the first and third bit lines is output from the first memory cell on the second bit line and from the second memory cell on the fourth bit line.

5. (Amended) The apparatus of claim 1, wherein the first comparator circuit is comprised of a single comparator with a first input coupled to the first bit line and a second input coupled to the [second] third bit line, and wherein the second comparator circuit is comprised of a single comparator with a first input coupled to the second bit line and a second input coupled to the fourth bit line.

6. (Amended) The apparatus of claim 5, wherein the output of the first comparator is coupled to a first latch to store an indication that the voltage level on the first bit line differs substantially from the voltage level on the [second] third bit line, and wherein the output of the second comparator is coupled to a second latch to store an indication that the voltage level on the second bit line differs substantially from the voltage level on the fourth bit line.

7. (Amended) The apparatus of claim 6, wherein the time at which the [latch is] first and second latches are triggered is adjustable.

8. (Amended) The apparatus of claim 6, wherein the first latch is a sticky latch that is triggered to latch an indication that the voltage level on the first bit line differs substantially from the voltage level on the [second] third bit line, and wherein the second latch is a sticky latch that is triggered to latch an indication that the voltage on the third bit line differs substantially from the voltage on the fourth bit line [at any time that such an indication takes place].

9. (Amended) The apparatus of claim 1, wherein the first and second comparator [circuit is] circuits are each comprised of:

a subtracting circuit with a first input coupled to the first bit line and a second input coupled to the second bit line;

a first comparator coupled to the output of the subtracting circuit; and

a second comparator coupled to the output of the subtracting circuit.

14. (Amended) A method, comprising:

writing identical values to the first and second memory cells;

coupling a first memory cell to a first bit line;

coupling the first memory cell to a second bit line;

coupling a second memory cell to a [second] third bit line;

coupling the second memory cell to a fourth bit line;

coupling the first and [second] third bit lines to inputs of a first comparator circuit;

coupling the second and fourth bit lines to inputs of a second comparator circuit;

reading the identical values from the first memory cell through the first bit line and from the second memory cell through the [second] third bit line;

reading the identical values from the first memory cell through the second bit line and from the second memory cell through the fourth bit line that are complements of the values read through the first and third bit lines;

comparing the voltage levels on the first and [second] third bit lines; and

comparing the voltage levels on the second and fourth bit lines.

15. (Amended) The method of claim 14, further comprising latching an indication from the first comparator circuit of whether or not [that] the voltage level of the first bit line differs substantially from the voltage level of the [second] third bit line, and latching an indication from the second comparator circuit of whether or not the voltage level of the second bit line differs substantially from the voltage level of the fourth bit line.

16. (Amended) The method of claim 14, further comprising setting the degree to which the difference in voltage levels between the first bit line and the [second] third bit line, and between the second bit line and the fourth bit line [is] are substantial.